AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

Listing of Claims:

1. (Previously Presented) A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a first element forming region of a main surface of a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over a second element forming region of said main surface of said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film being thinner than said first gate insulating film,

wherein said first gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film and having a thickness greater than that of said thermally oxidized film,

wherein said second gate insulating film includes a thermally oxidized film,

wherein said first element forming region and said second element forming region are individually isolated by an element isolation region,

wherein said element isolation region is formed by forming grooves in said substrate, depositing an insulating film over said grooves by a vapor deposition

method, and polishing said insulating film so as to fill said insulating film in said grooves, and

wherein said deposited film extends over said element isolation region such that an edge portion of said first gate electrode is formed over said deposited film at a portion of said deposited film positioned over said element isolation region.

2. (Previously Presented) A semiconductor integrated circuit device according to claim 1, wherein an etching rate of said insulating film filled in said groove is lower than that of said thermally oxidized film.

3. (Original) A semiconductor integrated circuit device according to claim 1, wherein said deposited film is formed by a vapor deposition method.

4. (Previously Presented) A semiconductor integrated circuit device according to claim 3, wherein said vapor deposition method is a chemical vapor deposition method.

5. (Previously Presented) A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film of said second MISFET being thinner than said first gate insulating film,

wherein said first gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film and having a thickness greater than that of said thermally oxidized film,

wherein said second gate insulating film includes a thermally oxidized film,

wherein an insulating region having a thickness greater than that of said first gate insulating film is formed by forming grooves in said substrate, depositing an insulating film over said grooves by a vapor deposition method and polishing said insulating film so as to fill said insulating film in said grooves, and

wherein said deposited film extends over said insulating film such that an edge portion of said first gate electrode in a gate width direction thereof is formed over a portion of said deposited film positioned over said insulating film.

6. (Previously Presented) A semiconductor integrated circuit device according to claim 5, wherein an etching rate of said insulating film is filled in said groove is lower than that of said thermally oxidized film.

7. (Original) A semiconductor integrated circuit device according to claim 5, wherein said insulating film is integrally formed with an element isolation film defining a first MISFET forming region.

8. (Cancelled).

9. (Previously Presented) A semiconductor integrated circuit device according to claim 5, wherein said deposited film is formed by a vapor deposition method.

10. (Original) A semiconductor integrated circuit device according to claim 9, wherein said vapor deposition method is a chemical vapor deposition method.

11.-12. (Cancelled).

13. (Previously Presented) A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film of said second MISFET being thinner than said first gate insulating film,

wherein said first gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film and having a thickness greater than that of said thermally oxidized film,

wherein said second gate insulating film includes a thermally oxidized film,

wherein an insulating region having a thickness greater than that of said first gate insulating film is filled in a groove formed in said substrate by depositing an insulating film over said groove by a vapor deposition method and by polishing said insulating film so as to bury said insulating film in said groove,

wherein said insulating film is integrally formed with an element isolation film defining a first MISFET forming region,

wherein said deposited film extends over said insulating film such that an edge portion of said first gate electrode is formed over said deposited film at a portion of said deposited film positioned over said insulating film, and

wherein an etching rate of said insulating film filled in said groove is lower than that of said thermally oxidized film.

14. (Cancelled).

15. (Previously Presented) A semiconductor integrated circuit device according to claim 13, wherein said deposited film is formed by a vapor deposition method.

16. (Original) A semiconductor integrated circuit device according to claim 15, wherein said vapor deposition method is a chemical vapor deposition method.

17.-18. (Cancelled).

19. (Previously Presented) A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film of said second MISFET being thinner than said first gate insulating film,

wherein said first gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film,

wherein said second gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film and having a thickness thinner than that of said deposited film of said first gate insulating film,

wherein an insulating region having a thickness greater than that of said first gate insulating film is filled in a groove formed in said substrate by depositing an insulating film over said groove by a vapor deposition method and by polishing said insulating film so as to fill said insulating film in said groove, and

wherein said deposited film of said first gate insulating film extends over said insulating film such that said first gate electrode is formed over said deposited film of said first gate insulating film at a portion of said deposited film of said first gate insulating film positioned over said insulating film.

20. (Original) A semiconductor integrated circuit device according to claim 19, wherein said insulating film is integrally formed with an element isolation film defining a first MISFET forming region.

21. (Cancelled).

22. (Previously Presented) A semiconductor integrated circuit device according to claim 19, wherein said deposited film of said first gate insulating film is formed by a vapor deposition method.

23. (Original) A semiconductor integrated circuit device according to claim 22, wherein said vapor deposition method is a chemical vapor deposition method.

24. (Cancelled).

25. (Previously Presented) A semiconductor integrated circuit device according to claim 19, wherein said deposited film of said second gate insulating film is formed by a vapor deposition method.

26. (Original) A semiconductor integrated circuit device according to claim 25, wherein said vapor deposition method is a chemical vapor deposition method.

27. (Currently Amended) A method of manufacturing a semiconductor integrated circuit device, comprising steps ~~at~~of:

(a) depositing a first insulating film over a main surface, including a first element forming region and a second element forming region, of a semiconductor substrate;

(b) removing said first insulating film over said second element forming region;

(c) after said step (b), densifying said first insulating film; and

(d) forming a second insulating film over said second element forming region such that a thickness of said second insulating film is thinner than a thickness of said first insulating film,

wherein a first field effect transistor includes said first insulating film as a gate insulating film, and

wherein a second field effect transistor includes said second insulating film as a gate insulating film.

28. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 27, wherein said step (c) is a same step as said step (d).

29. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 27, wherein said step (d) is performed by thermally oxidizing said main surface to form a thermally oxidized film as said second insulating film.

30. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 27, wherein a separation region is provided between said first element forming region and said second element forming region, and wherein in said step (a) said first insulating film is formed over said separation region.

31. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 30, wherein said separation region is provided by forming a groove in said substrate, by burying a buried insulating film in said groove and by densifying said buried insulating film

32. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

(a) depositing a first insulating film over a main surface, including a first element forming region and a second element forming region, of a semiconductor substrate;

(b) removing said first insulating film over said second element forming region; and

(c) after said step (b), thermally oxidizing said main surface to form a second insulating film over said second element forming region such that a thickness of said second insulating film is thinner than a thickness of said first insulating film,

wherein a step of densifying said first insulating film is added at another step as said step (c),

wherein a first field effect transistor includes said first insulating film as a gate insulating film, and

wherein a second field effect transistor includes said second insulating film as a gate insulating film.

33. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 32, wherein a separation region is provided between said first element forming region and said second element forming region, and wherein in said step (a) said first insulating film is formed over said separation region.

34. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 33, wherein said separation region is provided by forming a groove in said substrate, by burying a buried insulating film in said groove and by densifying said buried insulating film.

35. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

(a) depositing a first insulating film over a main surface, including a first element forming region and a second element forming region, of a semiconductor substrate;

(b) removing said first insulating film over said second element forming region; and

(c) after said step (b), forming a second insulating film over said second element forming region such that a thickness of said second insulating film is thinner than a thickness of said first insulating film,

wherein a step of densifying said first insulating film is added at another step as said step (c),

wherein a first field effect transistor includes said first insulating film as a gate insulating film, and

wherein a second field effect transistor includes said second insulating film as a gate insulating film.

36. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 35, wherein a separation region is provided between said first element forming region and said second element forming region, and wherein in said step (a) said first insulating film is formed over said separation region.

37. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 36, wherein said separation region is provided by forming a groove in said substrate, by burying a buried insulating film in said groove and by densifying said buried insulating film.

38. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

(a) depositing a first insulating film over a main surface, including a first element forming region and a second element forming region, of a semiconductor substrate;

(b) removing said first insulating film over said second element forming region; and

(c) after said step (b), thermally oxidizing said main surface to form a second insulating film over said second element forming region such that a thickness of said second insulating film is thinner than a thickness of said first insulating film,

wherein a first field effect transistor includes said first insulating film as a gate insulating film, and

wherein a second field effect transistor includes said second insulating film as a gate insulating film.

39. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 38, wherein a separation region is provided between said first element forming region and said second element forming region, and wherein in said step (a) said first insulating film is formed over said separation region.

40. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 39, wherein said separation region is provided by forming a groove in said substrate, by burying a buried insulating film in said groove and by densifying said buried insulating film.

41. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

(a) depositing a first insulating film over a first element forming region and a second element forming region of a main surface of a semiconductor substrate, and over a second insulating film formed between said first element forming region and said second element forming region;

(b) removing said first insulating film over said second element forming region;

(c) after said step (b), thermally oxidizing said main surface to form a third insulating film over said second element forming region such that a thickness of said third insulating film is thinner than a thickness of said first insulating film,

wherein a first field effect transistor includes said first insulating film as a gate insulating film, and

wherein a second field effect transistor includes said third insulating film as a gate insulating film.

42. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 41, wherein said second insulating film is formed by forming a groove in said substrate, by burying a buried insulating film in said groove and by densifying said buried insulating film.

43. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

(a) depositing a first insulating film over a first element forming region and a second element forming region of a main surface of a semiconductor substrate, and over a second insulating film formed between said first element forming region and said second element forming region;

(b) removing said first insulating film over said second element forming region;

(c) after said step (b), densifying said first insulating film; and

(d) forming a third insulating film over said second element forming region such that a thickness of said third insulating film is thinner than a thickness of said first insulating film,

wherein a first field effect transistor includes said first insulating film as a gate insulating film, and

wherein a second field effect transistor includes said third insulating film as a gate insulating film.

44. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 43, wherein said second insulating film is formed by forming a groove in said substrate, by burying a buried insulating film in said groove and by densifying said buried insulating film.

45. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 43, wherein said step (c) is a same step as said step (d).

46. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 43, wherein said step (d) is performed by thermally oxidizing said main surface to form a thermally oxidized film as said third insulating film.

47. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

(a) depositing a first insulating film over a first element forming region and a second element forming region of a main surface of a semiconductor substrate, and over a second insulating film formed between said first element forming region and said second element forming region;

(b) removing said first insulating film over said second element forming region; and

(c) after said step (b), thermally oxidizing said main surface to form a third insulating film over said second element forming region such that a thickness of said third insulating film is thinner than a thickness of said first insulating film,

wherein a step of densifying said first insulating film is added at another step as said step (c),

wherein a first field effect transistor includes said first insulating film as a gate insulating film, and

wherein a second field effect transistor includes said third insulating film as a gate insulating film.

48. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 47, wherein said second insulating film serves as an element isolation region.

49. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

(a) depositing a first insulating film over a main surface, including a first element forming region, a second element forming region and a third element forming region, of a semiconductor substrate;

(b) removing said first insulating film over said second element forming region and said third element forming region;

(c) after said step (b), thermally oxidizing said main surface to form a second insulating film over both said second element forming region and said third element forming region such that a thickness of said second insulating film is thinner than a thickness of said first insulating film;

(d) after said step (c), removing said second insulating film over said third element forming region; and

(e) after said step (d), thermally oxidizing said main surface to form a third insulating film over said third element forming region such that a thickness of said third insulating film is thinner than a thickness of said second insulating film,

wherein a first field effect transistor includes said first insulating film as a gate insulating film,

wherein a second field effect transistor includes said second insulating film as a gate insulating film, and

wherein a third field effect transistor includes said third insulating film as a gate insulating film.

50. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 49, wherein a separation region is provided between said first element forming region, said second element forming region and said third element forming region, and wherein in said step (a) said first insulating film is formed over said separation region.

51. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 50, wherein said separation region is provided by forming a groove in said substrate, by burying a buried insulating film in said groove and by densifying said buried insulating film.

52. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

(a) depositing a first insulating film over a first element forming region, a second element forming region and a third element forming region of a main surface of a semiconductor substrate, and over a second insulating film formed between said first element forming region, said second element forming region and said third element forming region;

(b) removing said first insulating film over said second element forming region and said third element forming region;

(c) after said step (b), thermally oxidizing said main surface to form a third insulating film over both said second element forming region and said third element forming region such that a thickness of said third insulating film is thinner than a thickness of said first insulating film;

(d) after said step (c), removing said third insulating film over said third element forming region; and

(e) after said step (d), thermally oxidizing said main surface to form a fourth insulating film over said third element forming region such that a thickness of said fourth insulating film is thinner than a thickness of said third insulating film,

wherein a first field effect transistor includes said first insulating film as a gate insulating film,

wherein a second field effect transistor includes said third insulating film as a gate insulating film, and

wherein a third field effect transistor includes said fourth insulating film as a gate insulating film.

53. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 52, wherein said second insulating film is formed by forming a groove in said substrate, by burying a buried insulating film in said groove and by densifying said buried insulating film.

54. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

(a) depositing a first insulating film over a first element forming region, a second element forming region and a third element forming region of a main surface of a semiconductor substrate, and over a second insulating film formed between said first element forming region, said second element forming region and said third element forming region;

(b) removing said first insulating film over said second element forming region and said third element forming region;

(c) after said step (b), forming a third insulating film over both said second element forming region and said third element forming region such that a thickness of said third insulating film is thinner than a thickness of said first insulating film;

(d) after said step (c), removing said third insulating film over said third element forming region; and

(e) after said step (d), forming a fourth insulating film over said third element forming region such that a thickness of said fourth insulating film is thinner than a thickness of said third insulating film,

wherein a first field effect transistor includes said first insulating film as a gate insulating film,

wherein a second field effect transistor includes said third insulating film as a gate insulating film, and

wherein a third field effect transistor includes said fourth insulating film as a gate insulating film.

55. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device according to claim 54, wherein said second insulating film is

formed by forming a groove in said substrate, by burying a buried insulating film in said groove and by densifying said buried insulating film.

56. (Previously Presented) A semiconductor integrated circuit device according to claim 1, wherein said element isolation region is an insulating region having a thickness greater than that of said first gate insulating film.

57. (Previously Presented) A semiconductor integrated circuit device according to claim 56, wherein said insulating film is integrally formed with an element isolation film defining a first MISFET forming region, and wherein an etching rate of said insulating film filled in said groove is lower than that of a thermally oxidized film.

58. (New) A semiconductor integrated circuit device according to claim 1, wherein a thickness of said thermally oxidized film of said first gate insulating film is thinner than that of said thermally oxidized film of said second gate insulating film.

59. (New) A semiconductor integrated circuit device according to claim 5, wherein a thickness of said thermally oxidized film of said first gate insulating film is thinner than that of said thermally oxidized film of said second gate insulating film.

60. (New) A semiconductor integrated circuit device according to claim 13, wherein a thickness of said thermally oxidized film of said first gate insulating film is thinner than that of said thermally oxidized film of said second gate insulating film.

61. (New) A semiconductor integrated circuit device according to claim 19, wherein a thickness of said thermally oxidized film of said first gate insulating film is thinner than that of said thermally oxidized film of said second gate insulating film.

62. (New) A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a first element forming region of a main surface of a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over a second element forming region of said main surface of said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film being thinner than said first gate insulating film,

wherein said first gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film and having a thickness greater than that of said thermally oxidized film,

wherein said second gate insulating film includes a thermally oxidized film,

wherein said first element forming region and said second element forming region are individually isolated by an element isolation region,

wherein said element isolation region is formed by forming grooves in said substrate, by depositing an insulating film over said grooves by a vapor deposition method and by polishing said insulating film so as to bury said insulating film in said grooves, and

wherein a thickness of said thermally oxidized film of said first gate insulating

film is thinner than that of said thermally oxidized film of said second gate insulating film.

63. (New) A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a first element forming region of a main surface of a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over a second element forming region of said main surface of said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film being thinner than said first gate insulating film,

wherein said first gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film and having a thickness greater than that of said thermally oxidized film,

wherein said second gate insulating film includes a thermally oxidized film,

wherein said first element forming region and said second element forming region are individually isolated by an element isolation region, and

wherein said element isolation region is formed by forming grooves in said substrate, by depositing an insulating film over said grooves by a vapor deposition method and by polishing said insulating film so as to bury said insulating film in said grooves.

64. (New) A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a first element forming region of a main surface of a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over a second element forming region of said main surface of said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film being thinner than said first gate insulating film,

wherein said first gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film and having a thickness greater than that of said thermally oxidized film,

wherein said second gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film of the second gate insulating film,

wherein said first element forming region and said second element forming region are individually isolated by an element isolation region, and

wherein said element isolation region is formed by forming grooves in said substrate, by depositing an insulating film over said grooves by a vapor deposition method and by polishing said insulating film so as to bury said insulating film in said grooves.

65. (New) A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a first element forming region of a main surface of a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over a second element forming region of said main surface of said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film being thinner than said first gate insulating film,

wherein said first gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film and having a thickness greater than that of said thermally oxidized film, and

wherein said second gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film of the second gate insulating film.

66. (New) A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a first element forming region of a main surface of a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over a second element forming region of said main surface of said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film being thinner than said first gate insulating

film,

wherein said first gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film,

wherein said second gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film of the second gate insulating film, and having a thickness greater than that of said thermally oxidized film of the second gate insulating film,

wherein said first element forming region and said second element forming region are individually isolated by an element isolation region, and

wherein said element isolation region is formed by forming grooves in said substrate, by depositing an insulating film over said grooves by a vapor deposition method and by polishing said insulating film so as to bury said insulating film in said grooves.

67. (New) A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a first element forming region of a main surface of a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over a second element forming region of said main surface of said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film being thinner than said first gate insulating film,

wherein said first gate insulating film includes a thermally oxidized film and a

deposited film formed over said thermally oxidized film, and

wherein said second gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film and having a thickness greater than that of said thermally oxidized film of said second gate insulating film.

68. (New) A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a first element forming region of a main surface of a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over a second element forming region of said main surface of said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film being thinner than said first gate insulating film,

wherein said first gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film and having a thickness greater than that of said thermally oxidized film,

wherein said second gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film of the second gate insulating film, and having a thickness greater than that of said thermally oxidized film of the second gate insulating film,

wherein said first element forming region and said second element forming region are individually isolated by an element isolation region, and

wherein said element isolation region is formed by forming grooves in said

substrate, by depositing an insulating film over said grooves by a vapor deposition method and by polishing said insulating film so as to bury said insulating film in said grooves.

69. (New) A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a first element forming region of a main surface of a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over a second element forming region of said main surface of said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film being thinner than said first gate insulating film,

wherein said first gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film and having a thickness greater than that of said thermally oxidized film, and

wherein said second gate insulating film includes a thermally oxidized film and a deposited film formed over said thermally oxidized film of the second gate insulating film, and having a thickness greater than that of said thermally oxidized film of the second gate insulating film.